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1) **GERENAL SPECIFICATION**

**The LCD module OD-M643A is used to display 8-digit 14 seg alphanumeric. It has wide viewing angle, wide temperature range and low power consumption.**

**2) FEATURES**

- Operating voltage : 4.8V-5.2V
- A built-in 256KHz RC oscillator
- Selection of 1/3 bias, and selection of 1/4 duty LCD applications
- Internal time base frequency sources
- Power down command to reduce power consumption
- A 32 X 4 LCD driver
- A built-in 32 X 4 bit display RAM
- Four-line serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instruction
- Three data accessing modes
- Provide VLCD pin for adjusting LCD operating voltage

**3) ABSOLUTE MAXIMUM RATINGS**

Supply Voltage.....-0.3V-5.5V                      Storage Temperature.....-50C-125C.  
 Input Voltage .....Vss-0.3V-Vdd+0.3V            Operating Temperature..... -25C-75C

\*Note: Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operationa sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Interface definition

Pin No.	Symbol	Description
1	$\overline{\text{CS}}$	Chip selection input with a pull-high resistor. When the CS is logic high, the data and command read from or written to the HT1621 are disabled. The serial interface circuit is also reset. But if the CS is at a logic low level and is input to the CS pad, the data and command transmission between the host controller and the HT1621 are all enabled.
2	$\overline{\text{RD}}$	READ clock input with a pull-high resistor Data in the RAM of the HT1621 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next raising edge to latch the clocked out data.
3	$\overline{\text{WR}}$	WRITE clock input with a pull-high resistor Data on the DATA line are latched into the HT1621 on the rising edge of the WR signal.
4	DATA	Serial data input/output with a pull-high resistor
5	Vss	I Negative power supply, GND
6	VLCD	LCD power input
7	VDD	Positive power supply
8	A	Power supply for LED+
9	K	Power supply for LED-

#### 4) ELECTRICAL SPECIFICATION

##### 4.1 D.C. Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	—	2.4	—	5.2	V
IDD	Operating Current	No load On-chip RC oscillator	—	300	600	μA
ISTB	Standby Current	Power down mode	—	0.3	10	μA
VIL	Input Low Voltage	DATA, WR, CS, RD	0	—	1.0	V
VIH	Input High Voltage	DATA, WR, CS, RD	4.0	—	5.0	V
IOL1	DATA	VOL=0.5V	1.3	2.6	—	mA
IOH1	DATA		-0.9	-1.8	—	mA
RPH	Pull-High Resister	DATA, WR, CS, RD	30	60	100	kΩ

##### 4.2 A.C. Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
fSYS	System Clock	On-chip RC oscillator	—	256	—	kHz
fLCD	LCD Clock	On-chip RC oscillator	—	fSYS/1024	—	kHz
tCOM	LCD Common Period	n: Number of COM	—	n/fLCD	—	
fCLK1	Serial Data Clock (WR pin)	Duty cycle 50%	—	—	300	kHz
fCLK2	Serial Data Clock (RD pin)	Duty cycle 50%	—	—	150	kHz
fTONE	Tone Frequency	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
tCS	Serial Interface Reset Pulse	CS	—	250	—	ns
tw	Pulse Width Serial Data	Read mode Write mode	1.67 3.34	—	—	μs
trtf	Rise/Fall Time Serial Data	—	—	120		ns
tsu	Setup Time DATA to Serial Data Clock	—	—	120		ns
th	Hold Time DATA to Serial Data Clock	—	—	120		ns

Symbol	parameter	Test Conditions	Min.	Typ.	Max	Unit
$t_n$	Low to CS High Serial Data Clock	—	—	100	—	ns
$t_{rec}$	CS High to Serial Data Clock	—	—	100	—	ns
$t_w$	Serial Interface Reset High	—	—	250	—	ns
$t_{su}$	CS Low to Serial Pulse Width	—	—	100	—	ns

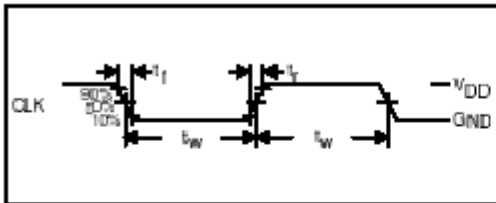


Figure 1.

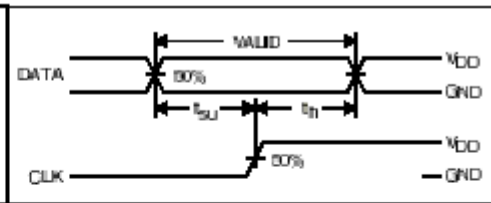


Figure 2.

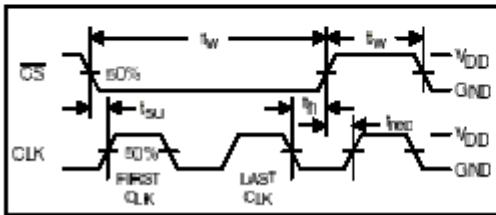


Figure 3.

## 5) System Architecture

### Display memory - RAM

The static display memory (RAM) is organized into 32'4 bits and stores the displayed data.

The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the

RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
SEG31					31
	Bit 3	Bit 2	Bit 1	Bit 0	Addr Bit

RAM Mapping

### System Oscillator

The HT1621 system clock is used to generate the time base/watch dog timer (WDT) clock frequency,

LCD driving clock, and tone frequency.

The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system

oscillator is as shown. After the SYS DIS command is executed, the system clock will stop

and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system.

### Command format

There are two mode commands to configure the LCM resources and to transfer the LCD display data. The configuration mode of the LCM is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency

selection command, an LCD configuration command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

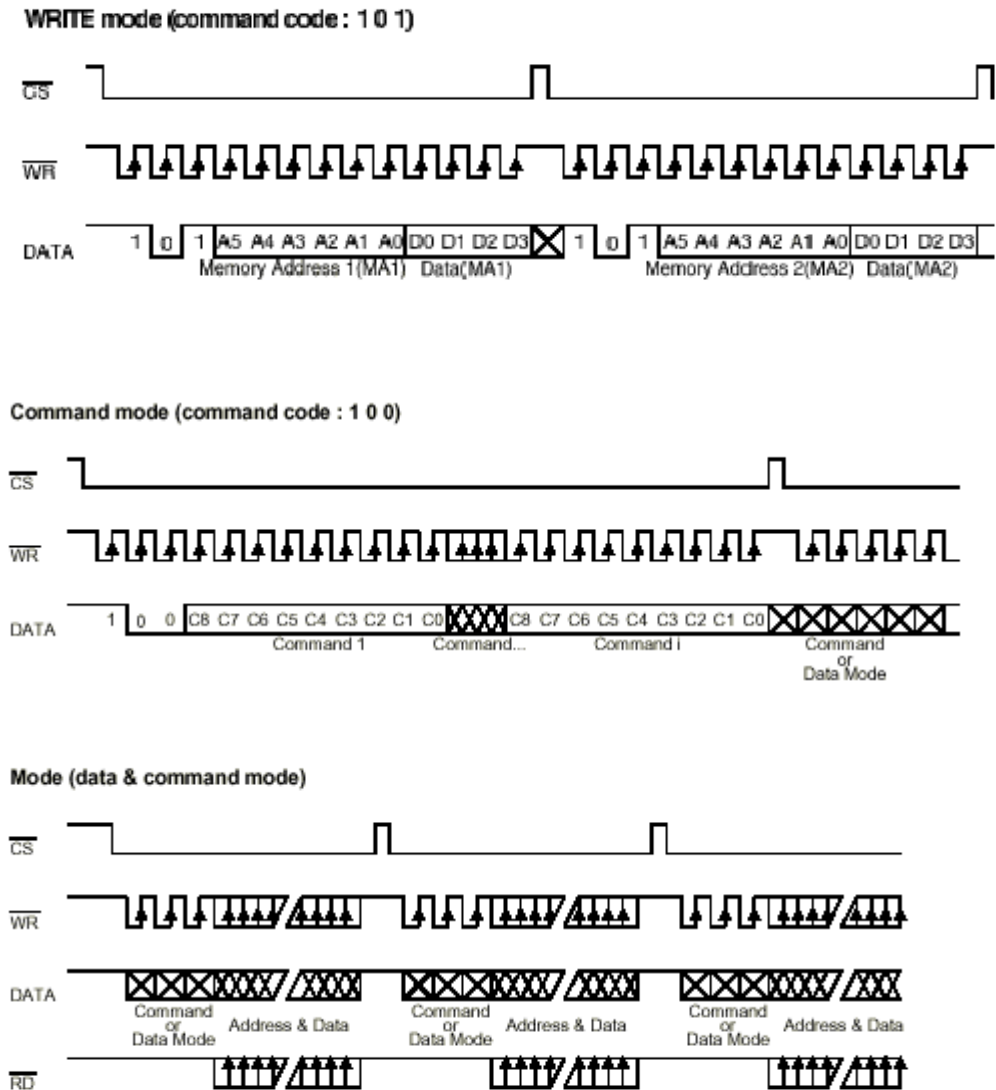
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to "1" and the previous operation mode will be reset also. Once the CS pin returns to "0", a new operation mode ID should be issued first.

**Interfacing**

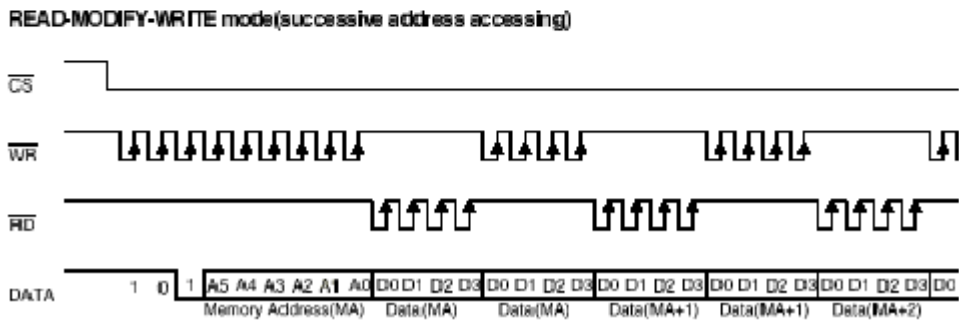
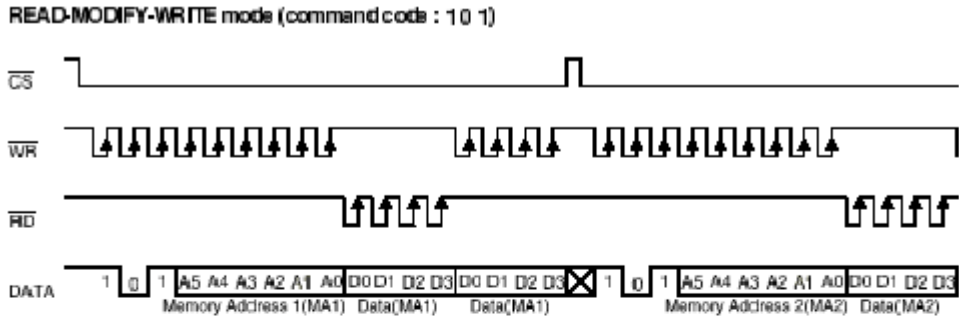
Only 4 lines are required to interface with the LCM. The CS line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the LCM. If the CS pin is set to 1, the data and command issued between the host controller and the LCM are first disabled and then initialized. Before issuing a mode command or mode switch-ing, a high level pulse is required to initialize the serial interface of the LCM. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be

passed through the DATA line. The RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the RD signal. The WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the LCM on the rising edge of the WR signal.

**6) TIMING DIAGRAM**



**Note:** It is suggested that the host controller should read in the data from the DATA line between the raising edge of the RD line and the falling edge of the next RD line.



## 7) Command Summary

Name	Command Code	D/C	Function	Power On ResetDefault
READ	a5 a4 a3 a2 a1 a0 d0 d1 d2 d3 101	D	Read data in the RAM	
WRITE	a5 a4 a3 a2 a1 a0 d0 d1 d2 d3 101	D	Write data t the RAM	
MODIFY	a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	READ and WRITE t the RAM	
SYS DIS	1 0 0 0 0 0 0 0 0 0 X	C	Turn off both system oscillator And LCD bias generator	
SYS EN	1 0 0 0 0 0 0 0 0 0 X	C	Turn on system oscillator	
LCD OFF	1 0 0 0 0 0 0 0 0 1 0 X	C	Turn off LCD bias generator	
LCD ON	1 0 0 0 0 0 0 0 0 1 1 X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0 0 0 0 0 0 1 0 0 X	C	Disable time base output	
TIMER EN	1 0 0 0 0 0 0 0 1 1 0 X	C	Enable time base output	
CLR TIMER	1 0 0 0 0 0 0 1 1 X X X	C	Clear the contents of time base generator	
RC 256K	1 0 0 0 0 0 1 1 0 X X X	C	System clock source, on-chip RC oscillator	
BIAS 1/3	1 0 0 0 0 1 0 a b X 1 X	C	ab=10:4 commons option	
TOPT	1 0 0 1 1 1 0 0 0 1 1 X	C	Test mode	
TNORMAL	1 0 0 1 1 1 0 0 0 1 1 X	C	Normal mode	



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**Note:**

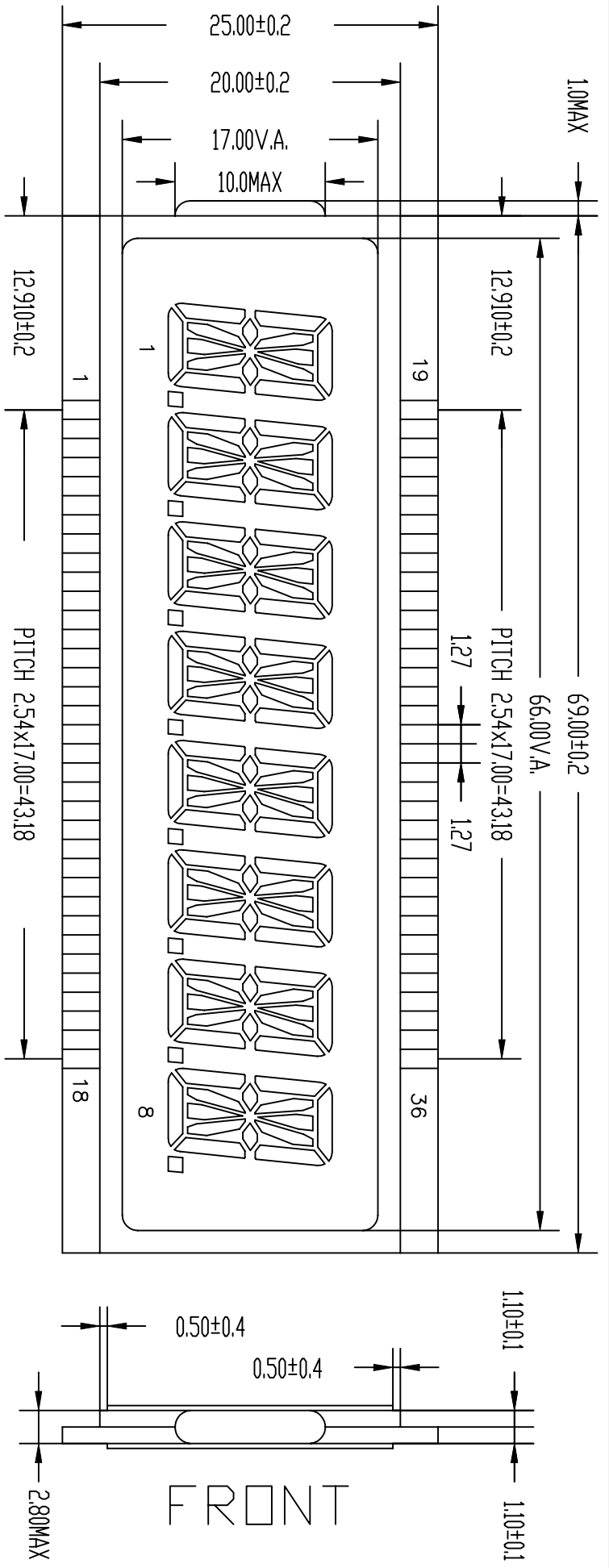
X : Don't care

a5~a0 : RAM addresses

d3~d0 : RAM data

D/C : Data/command mode

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except the first command will be omitted. It is suggested that the host controller should initialize the LCM after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the LCM.

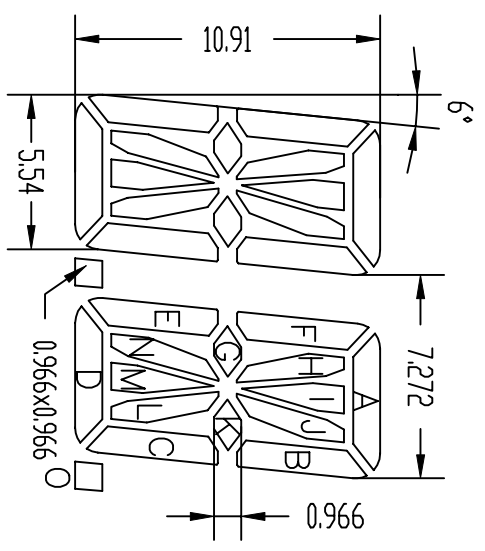


**SPECIFICATION:**

1.DRIVING VOLTAGE: 5.0V	6.DISPLAY MODE: POS, TN.
2.DRIVING METHOD: 1/4D, 1/3B	7.FRONT POLARIZER: TRANSMISSIVE.
3.STORAGE TEMP: -20°C TO 70°C	8.BACK POLARIZER: REFLECTIVE.
4.OPERATING TEMP: -10°C TO 60°C	9.CONNECTORS: NO PIN.
5.VIEWING ANGLE: 6H	10.SCREEN PRINTING: WITHOUT.

**ORIENT DISPLAY CO., LTD. 东显微电子**

TITLE: M643A	DESIGNER: XUYAN
UNIT: mm	CHECK:
SCALE:	APPROVER:
MODEL:	DATE: 2000-2-17
DATE: 2000-2-17	PAGE: 1 OF 2



LOGIC TABLE FOR M643A

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM0	1F	1A	1J	1B	2F	2A	2J	2B	3F	3A	3J	3B	4F	4A	4J	4B
COM1	1H	1I	1K	1C	2H	2I	2K	2C	3H	3I	3K	3C	4H	4I	4K	4C
COM2	1G	1N	1L	1D	2G	2N	2L	2D	3G	3N	3L	3D	4G	4N	4L	4D
COM3	1E	1M	1D		2E	2M	2D		3E	3M	3D		4E	4M	4D	
	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31
COM0	5F	5A	5J	5B	6F	6A	6J	6B	7F	7A	7J	7B	8F	8A	8J	8B
COM1	5H	5I	5K	5C	6H	6I	6K	6C	7H	7I	7K	7C	8H	8I	8K	8C
COM2	5G	5N	5L	5D	6G	6N	6L	6D	7G	7N	7L	7D	8G	8N	8L	8D
COM3	5E	5M	5D		6E	6M	6D		7E	7M	7D		8E	8M	8D	